In the Claims:

Please amend claims 1, 2, 3, 4, 5, 6, 7, 8, and 11-16 as follows:

1. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices in latch circuit designs including level sensitive scan design (LSSD) latches comprising the steps of:

identifying logic blocks in critical data and data clock paths of a L1 latch and a L2 latch of a LSSD latch ~~circuit~~;

substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor ~~for use~~ used in said identified logic blocks in the critical data and data clock paths of said L1 latch and said L2 latch of said LSSD latch; and

selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors.

2. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein said LSSD latch includes output buffer transistors, and further includes the steps of providing RVT transistors to implement said output buffer transistors.

3. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein said LSSD latch includes logic blocks used in loading data into said L1 latch of said LSSD latch and

wherein the step of identifying logic blocks in critical data and data clock paths ~~of the latch circuit~~ includes the steps of identifying said logic blocks used in loading data into said L1 latch of said LSSD latch ~~the latch circuit~~.

4. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 3 wherein said LSSD latch includes logic blocks used in each data clock stage of said LSSD latch and includes the steps of identifying said logic blocks used in each data clock stage.

5. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein said LSSD latch includes logic blocks used only during testing of said LSSD latch and wherein the step of selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying said logic blocks used only during testing of said LSSD latch ~~in the latch circuit~~; and selectively implementing ~~the identified~~ said logic blocks used only during testing only with RVT transistors, or low leakage (LLD) transistors.

6. (currently amended) A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein said LSSD latch includes logic blocks used to maintain the contents of latches of said LSSD latch and wherein the step of selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors includes the steps of

identifying logic blocks used to maintain the contents of latches of said LSSD latch ~~in the latch circuit~~; and selectively implementing ~~the identified~~ said logic blocks used to maintain the contents of latches only with RVT transistors, or low leakage (LLD) transistors.

7. (currently amended) A level sensitive scan design (LSSD) latch ~~circuit~~ for implementing enhanced performance with reduced quiescent power dissipation comprising:

critical data and data clock paths of a L1 latch and a L2 latch of the LSSD latch;

non-critical sections of said L1 latch and said L2 latch of the LSSD latch;

a low voltage threshold (LVT) transistor being used only in said critical data and data clock paths and implementing each transistor in said critical data and data clock paths of said L1 latch and said L2 latch of the LSSD latch; and

said non-critical sections being implemented only with regular voltage threshold (RVT) transistors, or low leakage (LLD) transistors.

8. (currently amended) A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said LSSD latch includes output buffer transistors, and includes said RVT transistors used for said output buffer transistors.

9. (original) A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said critical data and clock paths include multiple critical path logic blocks, each critical path logic block implemented with said LVT transistors.

10. (original) A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said non-critical sections include logic blocks used for testing and to maintain the contents of latches in the latch circuit.

11. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices in latch circuit designs including level sensitive scan design (LSSD) latches in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

identifying logic blocks in critical data and data clock paths of a L1 latch and a L2 latch of a LSSD latch ~~circuit~~;

substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor ~~for use~~ used in said identified logic blocks in the critical data and clock paths data clock paths of said L1 latch and said L2 latch of said LSSD latch; and

selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors.

12. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11

wherein said LSSD latch includes output buffer transistors, and further includes the steps of providing RVT transistors to implement said output buffer transistors.

13. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein said LSSD latch includes logic blocks used in loading data into said L1 latch of said LSSD latch and wherein the step of identifying logic blocks in critical data and data clock paths ~~of the latch circuit~~ includes the steps of identifying said logic blocks used in loading data into said L1 latch of said LSSD latch ~~the latch circuit~~.

14. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 13 wherein said LSSD latch includes logic blocks used in a data clock stage of said LSSD latch and includes the steps of identifying said logic blocks used in ~~a~~ said data clock stage..

15. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein said LSSD latch includes logic blocks used only during testing of said LSSD latch and wherein the step of selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying said logic blocks used only during testing of said LSSD latch ~~in the latch circuit~~; and selectively implementing ~~the identified~~ said logic blocks used only during testing only with RVT transistors, or low leakage (LLD) transistors.

16. (currently amended) A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein said LSSD latch includes logic blocks used to maintain the contents of latches of said LSSD latch and wherein the step of selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only ~~the latch circuit~~ with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used to maintain the contents of latches of said LSSD latch ~~in the latch circuit~~; and selectively implementing ~~the identified~~ said logic blocks used to maintain the contents of latches only with RVT transistors, or low leakage (LLD) transistors.